REMARKS

This Amendment is submitted in response to an Office action dated January 30, 2004, the shortened statutory period for response having expired on April 30, 2004. Accordingly, a Petition and Fee for Extension of Time are included herewith.

I. Status of the Claims

Claims 1-22 are pending in this application. The Examiner rejected all 22 pending claims in the Office action mailed on January 30, 3004. The Examiner also objected to claim 11.

II. Objection to Claim 11

The Examiner objected to claim 11 on the ground that the phrase "processing step the acquired image" is grammatically incorrect. Applicant has amended claim 11, and respectfully asks that the objection be withdrawn.

III. Rejections Under 35 U.S.C. § 102(e) – Dunton et al.

The Examiner rejected claims 11-13 and 16-17 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,556,242 to Dunton et al. ("Dunton et al."). *See* Office action at ¶ 3. Applicant respectfully traverses these rejections.

Claim 11 is directed to an electronic imager that includes a first and a second functional imaging subsystems, each imaging subsystem performing a processing step on the acquired image, the first imaging functional subsystem communicatively coupled to the second imaging functional subsystem and communicating to the second imaging functional subsystem an image data. This claim further includes an intermediate image storage buffer, communicatively coupled to the first and second imaging functional subsystems, the

intermediate storage buffer storing one or more image data communicated from the first imaging functional subsystem to the second imaging functional subsystem.

With regard to claim 11, the only independent claim among these rejected claims, the Examiner stated that Dunton et al.'s correction block 210 and scaling logic 214 at Fig. 2 correspond to claim 11's first and second functional imaging subsystems respectively, and that the RAM and/or LUT in Fig. 2 corresponds to the intermediate image storage buffer of claim 11.

Applicant respectfully submits that Dunton et al. fails to disclose or suggest an intermediate image storage buffer that is "communicatively coupled to the first and second imaging functional subsystems" and that "stor[es] one or more image data communicated from the first imaging functional subsystem to the second imaging functional subsystem," as is recited in claim 11. First, Dunton et al. indicates that the LUT and RAM described therein do not store images. As the specification of Dunton et al. explains, the LUT (or "look-up table") and RAM "provide information to its respective imaging function logic as specified by the selected methodology for the particular mode of operation." *See* Dunton et al. at col. 6, lines 28-43 and col. 2, lines 1-5. In other words, they only store parameters that are used for carrying out the logic for the correction or scaling of images, and not image data. Second, Fig. 2 of Dunton et al. indicates that neither the LUT, nor the RAM, are coupled to both the scaling logic 214 and the correction block 210. *See also* Dunton et al. at col. 6, lines 28-43 (stating that the LUT and RAM "provide information to its respective imaging function logic") (underlining added). Third, even though Dunton et al. discloses a local storage 122 for storing image data, the processing of images in Dunton et al. are performed before they are sent to that storage. *See* Dunton et al. at col. 4, lines 60-65 and Fig. 1.

Claims 12-13 and 16-17 depend on claim 11, and therefore are allowable for at least the reasons stated above because these claims include all of the features of claim 11. But Applicant also points out additional features of these dependent claims that are disclosed or suggested by Dunton et al.

Regarding claim 12, the Examiner states that Dunton et al.'s "original image data" and correction block 210 correspond to claim 12's raw image data and second imaging subsystem, respectively. But Dunton et al.'s LUT, as described above, does not store any images. Dunton et al. does not disclose or suggest an "intermediate image storage buffer storing one or more raw image data originating from the image interface circuitry" as recited in claim 12.

Regarding claim 13, the Examiner refers to Dunton et al.'s LUT as corresponding to the intermediate storage buffer of claim 13. But in Dunton et al., images are not communicated to the LUT, and there is no "signal" in response to which one or more images are communicated to the LUT. Therefore, Dunton et al. does not disclose or suggest claim 13's features that "one or more raw images are communicated to the intermediate storage buffer in response to a signal."

Regarding claim 16, the Examiner states that Dunton et al.'s correction block 210 and either the LUT or RAM of Dunton et al. correspond to claim 16's first imaging subsystem and intermediate image storage buffer respectively. However, if that were the case, then Dunton et al. does not disclose or suggest an "intermediate image storage buffer storing one or more processed image data originating from the image processing circuitry" as recited in claim 16 because Dunton et al.'s LUT or RAM, as described above, does not store any images.

Regarding claim 17, the Examiner refers to Dunton et al.'s LUT as corresponding to the intermediate storage buffer of claim 17. But in Dunton et al., images are not communicated to the LUT, and there is no "signal" in response to which one or more images are communicated to the LUT. Therefore, Dunton et al. does not disclose or suggest claim 17's features that "one or more processed images are communicated to the intermediate storage buffer in response to a signal."

For at least the reasons stated above, Applicant submits that Dunton et al. does not anticipate any of claims 11-13 and 16-17. Applicant thus respectfully requests that the rejections of these claims under 35 U.S.C. § 102(e) be withdrawn, and that the pending claims be allowed.

IV. Rejections Under 35 U.S.C. § 102(e) – Telle

The Examiner rejected claims 1-22 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,469,801 to Telle ("Telle"). *See* Office action at ¶ 4. Applicant respectfully traverses these rejections.

Claim 1 recites, among other things, image processing circuitry communicatively coupled to image sensing circuitry that processes raw image data into a processed image data, as well as a transformation circuitry communicatively coupled to the image processing circuitry that transforms the processed image data into a final image data. The Examiner has argued that the digital processing unit 52 in Fig. 2 of Telle simultaneously discloses both the image processing circuitry and the transformation circuitry of claim 1. Applicant respectfully submits that this is improper, for claim 1 recites imaging processing circuitry that is separate—and different—from its transformation circuitry so that it is possible to have an intermediate storage queue between the two. Consequently, Telle's digital processing unit 52 does not disclose or suggest both the image processing circuitry and the transformation circuitry of claim 1.

Claim 1 also recites, among other things, an intermediate storage queue, communicatively coupled to the image processing circuitry, that stores one or more image data "awaiting additional processing by the imaging system." In claim 1, the image data in the intermediate storage queue is not fully processed, hence it is "awaiting additional processing by the imaging system." In addition, all the raw data in the raw data storage of claim 1 goes to the image processing circuitry, and all the processed data in the processed data storage goes to the transformation circuitry. The reason for using the storage queue is to avoid, while processing a series of images, the need for processing each individual image through all of the various stages of the digital imaging system before processing the next individual image. *See* Applicant's specification at page 2, lines 9-15. By contrast, in Telle, the reason for having the buffers is to allow the user to view the image in the buffer to decide whether processing of a raw image or further processing of a modified image is desirable prior to printing the image. Thus, not all image data in Telle's buffers necessarily undergo processing. Moreover, to the extent an image in Telle's system is awaiting at all, it is awaiting the decision of the user to decide whether there will be additional processing, and is therefore not awaiting additional processing per se. *See* Telle, at col. 8, lines 5-25 and Fig. 2. Therefore, the buffers in Telle do not store one or more image data "awaiting additional processing by the imaging system" as recited in claim 1.

In addition, Applicant respectfully points out that the Examiner, in his rejection of claim 1, has referred to the buffer 56 of Telle as corresponding to the intermediate storage queue for the purpose of meeting one feature, and to the final storage for the purpose of meeting another feature. Claim 1 recites an intermediate storage queue and a final storage, and as such, the two cannot be the same.

Therefore, for each of the above reasons, Applicant respectfully submits that claim 1 is not anticipated by Telle.

Claims 2-9 depend on claim 1, and therefore are allowable for at least the reasons stated above because these claims include all of the features of claim 1. But Applicant also points out additional features of these dependent claims that are not disclosed or suggested by Telle.

Claim 3 recites, among other things, the holding of one or more raw image data in an intermediate storage queue while the image processing circuitry is processing another image data. Telle discloses an imaging system that is capable of handling and processing only one acquired image at a time—although the image data of the same acquired image may be altered more than once by processing. Thus, the system in Telle cannot hold one or more acquired image in an intermediate storage queue while an image processing circuitry is processing another acquired image, as is recited in claim 3.

Regarding claim 4, Applicant respectfully notes that the portions of Telle cited by the Examiner merely discuss image processing functions and do not disclose or suggest either the storing of additional raw image data in an intermediate storage queue, or delivering each raw image data stored in the intermediate storage queue upon the amount of raw image data in the intermediate storage queue reaching a predetermined level.

The system in Telle does not disclose or suggest storing of additional raw image data into an intermediate storage queue, for as discussed above, the system in Telle is not able to handle and process more than one acquired image at a time. In addition, the system in Telle does not disclose or suggest delivering of each raw image data stored in the intermediate storage queue upon the amount of raw image data in the intermediate storage queue reaching a

predetermined level, for it does not set any predetermined level in connection with the amount of raw image data in a storage, and does not have a mechanism for prompting delivery of the raw image data in the storage based on whether the amount in the storage exceeds such a predetermined level.

Claim 6 recites, among other things, the holding of one or more processed image data in an intermediate storage queue while the transformation circuitry is processing another image data. Telle discloses an imaging system that is capable of handling and processing only one acquired image at a time—although the image data of the same acquired image may be altered more than once by processing. Thus, the system in Telle cannot hold one or more acquired image in an intermediate storage queue while a transformation circuitry is processing another acquired image, as is recited in claim 6.

Regarding claim 7, Applicant respectfully notes that the portions of Telle cited by the Examiner merely discuss image processing functions and do not disclose or suggest either storing processed image data into an intermediate storage queue, or delivering each processed image data stored in the intermediate storage queue upon the amount of processed image data in the intermediate storage queue reaching a predetermined level. The system in Telle does not disclose or suggest storing of additional processed image data into an intermediate storage queue, for as above, the system in Telle does not have the ability to handle and process more than one acquired image at a time. In addition, the system in Telle does not disclose or suggest delivering each processed image data stored in the intermediate storage queue upon the amount of processed image data in the intermediate storage queue reaching a predetermined level, for it does not set any predetermined level in connection with the amount of processed image data in a

storage, and does not have a mechanism for prompting delivery of the processed image data in the storage based on whether the amount in the storage exceeds such a predetermined level.

Regarding claim 9, Applicant respectfully notes that there is no indication in Telle that the logic and control hardware 46 or the image processing block in Fig. 2 of Telle monitors the status of the buffers.

Regarding claim 10, although Figure 2 of Telle appears to disclose a power source, there is no indication that Telle's system processes the image data in its buffers in response to an indication that the system has been linked to the power source. And there is no indication in Telle of a connection between the processing of image data in storage and any linkage of the system to an external power source.

For these additional reasons, Applicant respectfully submits that claims 2-9 are not anticipated by Telle.

Independent claim 11 recites an imager that comprises a first and a second functional imaging subsystem that perform a processing step, as well as an intermediate storage buffer that is communicatively coupled to the first and second functional imaging subsystems. The Examiner, in rejecting claim 11, states that the CCD and Analog Front End Electronics 50 constitute a "first functional imaging subsystem." However, the CCD and Analog Front End Electronics 50 do not process image data. In Telle's imager, the digital image processing 52 performs the processing of image data. Therefore, the CCD and Analog Front End Electronics 50 cannot be a first functional imaging subsystem that performs a processing step, as is recited in claim 11. Consequently, Telle also does not disclose or suggest two functional imaging subsystems that are coupled to each other, an intermediate image storage buffer coupled to two

imaging functional subsystems, or an intermediate storage buffer that stores image data communicated from one imaging subsystem to another, as is recited in claim 11.

Claims 12-19 depend on claim 11, and therefore are allowable for at least the reasons stated above because their claims include all of the features of claim 11. But Applicant also points out additional features of these dependent claims that are also not disclosed or suggested by Telle.

Regarding claim 13, it appears that the CCD and Analog Front End Electronics 50 in Telle sends all the raw image data to the buffer 54 automatically and not in response to a particular signal. Hence there is no indication in Telle that its imager has a "signal," as is recited in claim 13.

Regarding claim 14, Telle does not disclose or suggest an imager wherein raw image data is sent to a memory storage based upon the meeting of certain conditions, and also does not disclose or suggest comparing the speed of the image interface circuitry with that of the processing circuitry. Thus, Telle does not disclose or suggest a signal that indicates that the image interface circuitry is producing a raw image at a faster rate that the processing circuitry can process the raw image, as is recited in claim 14.

Regarding claim 15, Telle does not disclose or suggest an imager wherein raw image data is sent to a memory storage based upon the meeting of certain conditions, and also does not disclose or suggest setting a predetermined amount regarding the amount of raw image data in an intermediate storage buffer and comparing that amount with the actual amount in that storage. Thus, Telle does not disclose or suggest a signal that indicates that the intermediate storage buffer contains less than a predetermined amount of raw image data, as is recited in claim 15.

Regarding claim 17, it appears that the digital image processor 52 in Telle sends all the processed image data to the buffer 56 automatically, and not in response to a particular signal. Hence there is no indication in Telle that its imager has a "signal," as is recited in claim 17.

Regarding claim 18, Telle does not disclose or suggest an imager wherein processed image data is sent to a memory storage based upon the meeting of certain conditions, and also fails to disclose or suggest comparing the speed of the image processing circuitry with that of the transformation circuitry. Thus, Telle does not disclose or suggest a signal that indicates that the image processing circuitry is producing a processed image at a faster rate that the transformation circuitry can process the processed image, as is recited in claim 18.

Regarding claim 19, Telle does not disclose or suggest an imager wherein processed image data is sent to a memory storage based upon the meeting of certain conditions, and also fails to disclose or suggest setting a predetermined amount regarding the amount of processed image data in an intermediate storage buffer and comparing that amount with the actual amount in that storage. Thus, Telle does not disclose or suggest a signal that indicates that the intermediate storage buffer contains less than a predetermined amount of processed image data, as is recited in claim 19.

Independent claim 20 recites a method comprising acquiring an initial image in an image sensor, producing a first image data from the initial image in the interface circuitry, processing the first image data into a second image data, and selectively storing the first image data in a buffer based on whether the processing is already operating on a previously communicated first image data.

First, the Examiner in rejecting claim 20 referred to item 54 in Telle's Fig. 2 when discussing the "producing" feature. By doing so, the Examiner seemed to suggest that Telle's item 54, which is a buffer, constitutes an interface circuitry that produces a first image data. However, the buffer of Telle does no such thing. Second, the Examiner also suggest that Telle's item 50, a CCD and Analog Front End Electronics, constitutes an image sensor that acquires an initial image. However, by doing so, the Examiner has attributed the same raw image data in Telle as being both an initial image as well as a first image data of claim 20. This is incorrect, for claim 20 clearly indicates that its initial image and first image data are not the same. Third, the portions of Telle the Examiner cited to do not disclose or suggest selectively storing image data based on some sort of a determination process, and therefore Telle does not disclose or suggest "selectively storing the first image data in a buffer based on whether the step of processing is already operating on a previously communicated first image data," as is recited in claim 20.

Claims 21-22 depend on claim 20, and therefore are allowable for at least the reasons stated above because these claims include all of the features of claim 20. But Applicant also points out that Telle does not disclose or suggest the transformation circuitry that is recited in each of claims 21 and 22.

For at least the reasons stated above, Applicant submits that Telle does not anticipate any of claims 1-22. Applicant thus respectfully asks the Examiner to withdraw the rejections of these claims under 35 U.S.C. § 102(e) and to allow the pending claims.

V. Conclusion and Request for Reconsideration

Applicant requests reconsideration of the present application in view of the aforementioned amendment and remarks. Although other features of the claims in the present

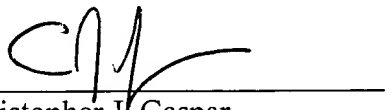
application are also significant, Applicant respectfully submits that the pending claims are allowable for at least the aforementioned reasons. Accordingly, Applicant respectfully requests that the rejections under § 102(e) be withdrawn, and that the pending claims be allowed.

In the event that a telephone conference would advance examination of this application, the Examiner is invited to contact the undersigned at the number provided.

VI. Authorization

Applicant respectfully submits herewith a Petition for Extension of Time (3 months), and a check in the amount of $950.00. In the event that the Commissioner determines that an additional extension of time or additional fee is due for this paper, the undersigned hereby petitions for any required extension of time, and authorizes the Commissioner to charge any fee required to Milbank's deposit account no. 13-3250, order no. 37213-03100. A DUPLICATE COPY OF THIS PAGE IS ENCLOSED HEREWITH.

Respectfully submitted,
Milbank, Tweed, Hadley & McCloy LLP



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